Appl. No. 09/943,714 Amdt. Dated 08/12/2005 Reply to Office Action of June 17, 2005

Amendments to the Specification:

Please replace paragraph [0002] with the following amended paragraph:

[0002] Direct modulation transmitter architecture, in which no intermediate frequency stage is utilized, in is finding increased popularity. A significant application is in cell phones and other wireless devices operating, for example, in the area of 1.9GHZ. Direct modulation architecture is of interest because of its simplicity and lower number of external circuit components such as surface acoustic wave (SAW) filters and voltage control oscillators (VCOs). Also, since there are not no intermediate frequency stages, the stages need not be driven. Consequently, the direct modulation transmitter provides for decreased power requirements. Efforts at integrating as many components as possible of a direct conversion transceiver onto a single chip have further led to increase increased popularity.

Please replace paragraph [0004] with the following amended paragraph:

[0004] One prior art approach to address these problems is <u>by</u> modulating on a sub-harmonic of the RF carrier frequency and <u>perform-performing</u> signal control on the sub-harmonic frequency. Then, the sub-harmonic frequency is multiplied, and the signal control is also performed on signals at the desired frequency. This approach increases dynamic range.

Please replace paragraph [0007] with the following amended paragraph:

[0007] It is a further object of the present invention to provide, in a direct modulation transmitter, signal processing at a first frequency level for a signal to be transmitted and increasing frequency to transmission frequency in a manner to avoid distortion.

Please replace paragraph [0010] with the following amended paragraph:

[0010] The means by which the foregoing objects and features of invention are achieved are pointed with particularity in the claims forming the concluding portion of the specification. The invention, both as to its organization and manner of operation, maybe may be further understood in reference to the following description taken in connection with the following drawings.

Please replace paragraph [0014] with the following amended paragraph:

[0014] Figure 1 is a block diagram illustrating a direct conversion transmitter instructed constructed in accordance with the present invention. A signal source 10 provides I&Q inputs to input terminals 13 and 14 of a digital signal processor 15. Signal source 10 maybe may be a well known source providing data, voice information or both. The I&Q signals provided to the terminals 13 and 14, respectively, are generated in baseband processing with the processor 15 performs performing a square root operation on the I&Q signals.

Docket No: 2661P055 Page 2 of 11 RWB/jc

Appl. No. 09/943,714 Amdt. Dated 08/12/2005 Reply to Office Action of June 17, 2005

Please replace paragraphs [0017]-[0019] with the following amended paragraphs:

- [0017] The square root of I and square root of Q outlets are fed to a conventional Gilbert cell modulator 18. Local oscillator 20 of the modulator 18 has a frequency of half of the desired transmitter frequency. A variable gain amplifier 22 at the output of the modulator 18 is also processing a signal at half of the desired transmitter frequency. The variable gain amplifier 22 provides an adjustable signal level, i.e., a signal of pre-selected power. the The output of the variable gain amplifier 22 is provided to a squaring circuit 26, further illustrated in Figure 2. As seen in Figure 2, the squaring circuit 26 is a Gilbert multiplier. The output of the variable gain amplifier is x(t). The input is divided into first and second inputs x1 and x2 of the squaring circuit 26. The squaring circuit 26 provides an output of the form y=x1 · x2=x².
- [0018] The result of the squaring operation <u>is</u> a signal <u>of on</u> the output of squaring circuit 26 which is the square of the input signal. The squaring operation also provides a <u>de-DC</u> component which is eliminated by a <u>de-DC</u> blocking capacitor 64 at the output of the squaring circuit 60. The output of the form w=x² has a frequency which is double the frequency of x and which is the desired transmission signal frequency.
- [0019] The control range of the signal output level is proportional to the square of the control range in the variable gain amplifier 22. Square-The square of the first signal is double the value of the first signal expressed in dB. A-After filtering in filter 66, a second variable gain amplifier 68 amplifies the radio frequency output from the squaring circuit 26. Conventional filtering means 70 are connected between the output of the variable gain amplifier 68 and a power amplifier 7072. The output of the power amplifier 70-72 is provided for transmission by an antenna 7274. In the present illustration, the antenna 72-74 is also intended to include impedance matching circuits.

Please replace paragraph [0021] with the following amended paragraph:

[0021] Distortions due to feedback inherent in circuitry of the modulator 18 are considerably lower because the IQ modulator 18 does not work on the same frequency as the transmitted frequency. Additionally, local oscillator pulling and/or inject locking is also significantly improved because the local oscillator does not work on the same frequency as the output signal from the transmitter. High control range of the output is provided while distortion is avoided.

Docket No: 2661P055 Page 3 of 11 RWB/jc